Claims

1. A method for fabricating a nanoscale or atomic scale device, comprising the steps of:

creating one or more registration markers visible to a Scanning Tunnelling Microscope (STM), Scanning Electron Microscope (SEM) or an optical microscope, on or in a (clean) silicon surface;

using a SEM or optical microscope to form an image of at least one of the registration markers and the tip of a Scanning tunnelling Microscope (STM) in the vicinity of the registration marker;

using the image to position and reposition the STM tip relative to the marker with nanometre or micron resolution in order to pattern the active region of the device structure on the silicon surface;

the device and then encapsulating it with silicon such that one or more of the registration markers are still visible on the silicon surface to a SEM or optical microscope;

depositing a metal layer onto the silicon surface using either optical or electron beam lithography to form one or more ohmic or gate electrodes, or both, at one or more locations positioned relative to respective registration markers.

2. A method according to claim 1, wherein the silicon surface is the (100)-oriented surface having a 2x1 unit cell surface structure with rows of σ-bonded silicon dimers.

3. A method according to claim 1 or 2, wherein the silicon surface is up to $1cm^2$ in size.

4. A method according to any preceding claim, wherein the registration markers are defined by optical or e-beam lithography (EBL).

5. A method according to any preceding claim, wherein the registration markers are created using focussed ion beam (FIB) milling or etching of the silicon surface.

6. A method according to any one of claims 1 to 4, wherein the registration markers are created using wet-chemical etching or reactive ion etching (RIE).

7. A method according to any one of claims 1 to 4, wherein the registration markers are created by depositing metal onto the silicon surface.

8. A method according to any preceding claim, wherein the markers are sized between a few nm and several microns.

9. A method according to any preceding claim, wherein a series of registration marker of different sizes and patterns are created to form a target around a selected site for the nanoscale device.

10. A method according to claim 9, wherein the smallest marker ranges from tens to several hundred nanometers in diameter.

11. A method according to any preceding claim, wherein the registration markers are from tens to several hundred nanometers deep.

12. A method according to any preceding claim, wherein after creating the markers the silicon surface is cleaned to remove any traces or organic resists before loading into the STM vacuum system.

13. A method according to any preceding claim, wherein a laser interferometer stage is used to assist with repositioning of the STM over millimetre distances with nanometre resolution.

14. A method according to any preceding claim, wherein the structure is patterned by selectively desorbing atoms from a hydrogen monolayer on a silicon surface.

15. A method according to claim 14, wherein the exposed silicon is subsequently doped by exposure to gas atoms or molecules containing dopant atoms.

16. A method according to claim 15, wherein dopant atoms are activated by annealing the surface at between about 300^0C and about 650^0C to incorporate electrically active dopant atoms into the silicon.

17. A method according to claim 16, wherein the hydrogen monolayer is removed by annealing at $\sim 470 \pm 30$°C for less than 10 seconds.

18. A method according to claim 15, wherein annealing takes place at about 530°C for about 5 seconds.

19. A method according to claim 16, wherein the hydrogen monolayer is removed using the STM tip.

20. A method according to claim 16, wherein the hydrogen monolayer is removed using the SEM.

21. A method according to any one of the preceding claims, wherein encapsulating layers are epitaxially grown at between about 0^0C and 400^0C.

22. A method according to claim 21, wherein the encapsulating layers are grown at between about 0^0C and 250^0C.

23. A method according to claim 22, wherein the encapsulating layers are grown at room temperature.

24. A method according to any one of the preceding claims, wherein the encapsulating layers between 5 and several hundred nm thick.

25. A method according to any one of the preceding claims, including the further step of: thermally annealing the surface so that it becomes atomically smooth.

26. A method according to any preceding claim, including the further step of forming highly-doped gate regions close to and in the plane of the patterned device structure.

27. A method according to claim 26, including the further steps of: depositing metal layers on the silicon surface at locations positioned above respective highly-doped regions and then annealing to diffuse the metal down to the highly-doped regions.

28. A method according to claim 27, wherein the anneal is conducted at a sufficiently low temperature that significant dopant diffusion does not occur.

29. A method according to any one of claims 1 to 25, including the further step of implanting dopants to create a doped region extending from the surface down to the layer of the patterned device structure.

30. A method according to any preceding claim, including the further step of forming a three dimensional device by patterning a first layer of the device structure, then forming that device layer and overgrowing with one or more layers of silicon atoms and patterning the new surface with another layer of the device structure.

31. A method according to any preceding claim, including the further step of measuring the electrical activity of the device.

32. A nanoscale or atomic scale device fabricated according to any preceding claim.

33. A device according to claim 32, comprising dopant atoms incorporated into the silicon surface form buried qubit sites and highly-doped gate regions adjacent respective qubit sites, wherein some regions are operable as control gates for the qubit; and other regions are operable as coupling electrodes to read-out the qubit, and electrodes on the silicon surface are positioned above respective highly-doped regions.